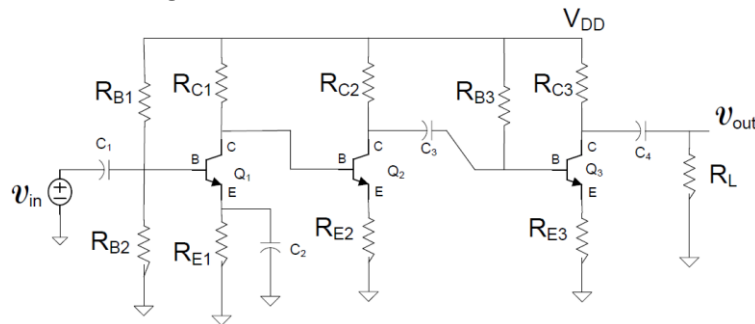


EE 330
 Homework 10
 Fall 2024
 Due Friday, Nov 1 at noon.

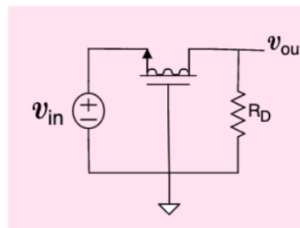
Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{ox} = 250 \mu\text{A}/\text{V}^2$ and $V_{Tn} = 0.4\text{V}$, all p-channel transistors have model parameters $\mu_p C_{ox} = \mu_n C_{ox}/3$ and $V_{Tp} = -0.4\text{V}$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14}\text{A}/\mu^2$ and $\beta = 100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14}\text{A}/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100 \mu^2$. Assume all diodes are characterized by the model parameters $J_{SX} = 0.5\text{A}/\mu\text{m}^2$, $V_{G0} = 1.17\text{V}$, and $m = 2.3$.

Problem 1 Draw the small signal equivalent circuit of the circuit shown below. Do not calculate the gain. Assume all capacitors are large.

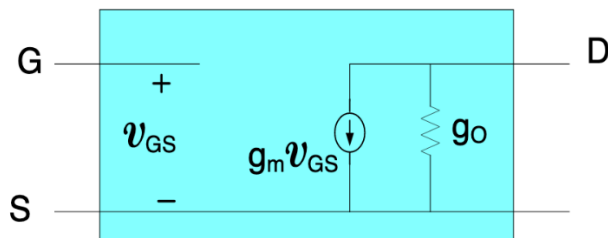


Problem 2 Assume the MOS transistor is operating in the saturation region and $\lambda = 0$ for the circuit shown.

- Find the small-signal voltage gain of the small-signal circuit shown in terms of the small-signal model parameters.
- Find the small-signal voltage gain of this circuit in terms of the quiescent operating point of the transistor



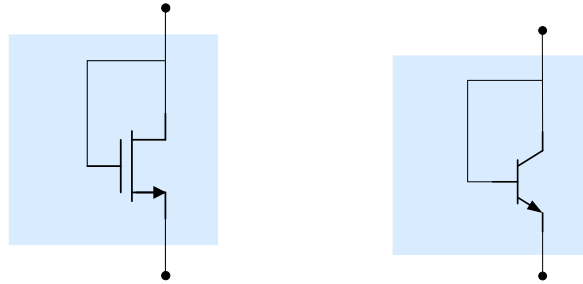
Problem 3 Recall from lecture that a saturated NMOS transistor can be modelled in the small-signal domain as follows:



where $g_m = \mu C_{ox} \frac{W}{L} (V_{GSQ} - V_T)$ and $g_o \approx \lambda I_{DQ}$. Derive the small-signal model of a PMOS device operating in the saturation region and compare with the model for the NMOS transistor.

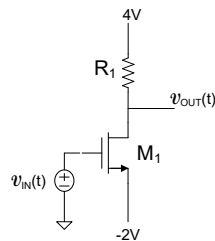
Problem 4 Consider the following circuits.

- Obtain the small signal impedance between the two terminals exiting the box in terms of the small-signal model parameters. Assume the MOSFET is operating in the Saturation region and the BJT in the Forward Active region
- These circuits are both one-port devices. Obtain the small-signal model for the two devices.
- Numerically determine the small-signal impedances if the quiescent currents are both 1mA, the width and length of the MOSFET are both $5\mu\text{m}$, and the emitter of the BJT is square and is $5\mu\text{m}$ on a side. Assume $V_{AF}=\infty$ and $\lambda=0$.

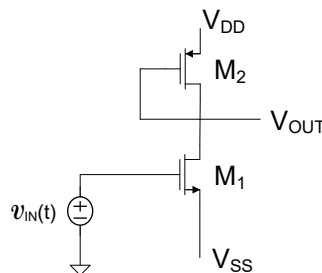


Problem 5

- Determine the maximum value of R_1 that will keep M_1 in saturation. M_1 has dimensions $W=18\mu$ and $L=2\mu$.
- If R_1 is $1/3$ of the value determined in Part a), determine the small signal voltage gain of this circuit
- With the value of R_1 used in part b), determine the total output voltage if $v_{IN}(t)=.001\sin(5000t+75^\circ)$.



Problem 6 Obtain an expression for the small signal output voltage in terms of the small signal parameters if the input is given by the expression $v_{IN}(t)=V_M\cos(\omega t+\theta)$. Assume M_1 is operating in the saturation region.

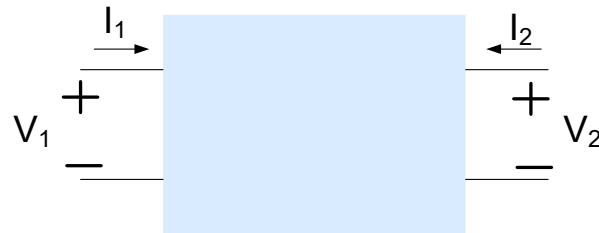


Problem 7 Design an amplifier using only MOS transistors, capacitors, and independent voltage sources that has a voltage gain of -10 when driving an external 10K resistor.

Problem 8 Consider a device characterized by the equations

$$I_1 = V_1 V_2^2$$

$$I_2 = 0.1e^{0.2V_1^2} V_2$$



- Determine the small signal model for a two-terminal device characterized by the equations given above
- Determine the numerical values for the small signal model parameters if the quiescent value of the port voltages are $V_2=1V$, $V_1=5V$.
- Determine the quiescent currents at the Q-point established in part b.
- Determine the small signal currents i_1 and i_2 if the small signal voltages v_1 and v_2 were measured to be $1mV_{RMS}$ and $2mV_{RMS}$ respectively. Assume the same Q-point as established in part b.

Problems 9 and 10 Implement a positive edge triggered D flip-flop with asynchronous reset and active low enable pin using Verilog. When the flip-flop is disabled or reset, its output should be low. Design a testbench proving function using Verilog. Submit module code, testbench code, and Modelsim waveforms.